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EXAMINER	
VERBRUGGE, KEVIN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,620	COULSON, RICHARD L.	
	Examiner	Art Unit	
	Kevin Verbrugge	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-14,16-26,28,29,31-37,40,41,43-46,48,49,51-55,57-60,77 and 82-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/17/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-8, 10-14, 16-26, 28-29, 31-37, 40-41, 43-46, 48-49, 51-55, 57-60, 77, and 82-106 .

DETAILED ACTION

Response to Amendment

This final Office action is in response to the amendment filed 7/26/05. Claims 1-8, 10-14, 16-26, 28-29, 31-37, 40-41, 43-46, 48-49, 51-55, 57-60, 77, and 82-106 remain pending. The rejection is repeated and made final because Applicant's arguments are not persuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 8, 16, 17, 19, 20, 21, 26, 28, 29, 31, 34, 35, 36, 37, 52, 58, 85, 87, 93, 96, 99, 101, 3, 4, 5, 32, 33, 6, 7, 10, 11, 22, 23, 12, 13, 24, 25, 44, 86, 89, 92, 100, 104, 14, 18, 53, 40, 41, 43, 45, 46, 48, 49, 51, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,860,083 to Sukegawa.

Regarding claims 1, 8, 16, 17, 19, 20, 21, 26, 28, 29, 31, 34, 35, 36, 37, 52, 58, 85, 87, 93, 96, 99, and 101, Sukegawa shows the claimed hard disk as hard disk drive (HDD) 2 in Fig. 1. He shows the claimed non-volatile cache memory as non-volatile

cache area 10C inside flash memory unit 1. He shows the claimed memory controller as cache system controller 3.

Sukegawa's memory controller determines if a memory request can be satisfied by accessing the non-volatile cache memory as claimed. If it can be satisfied by the cache (such as when a read request hits the cache), then it is satisfied by the cache (see column 7, lines 30-39). This is standard caching procedure.

If it cannot be satisfied by the cache (such as when new or updated data is written to the cache), then it is queued up for later execution (writing to the hard disk) as claimed (see column 10, lines 5-13).

Sukegawa does not teach that the queued up requests are executed when the hard disk is accessed in response to a read memory request (such as when a read misses the cache). He teaches that the queued up requests are executed when the storage area (queue) for updated data writes is full.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to execute queued up memory requests when the hard disk is accessed in response to a read memory request because this would further reduce the frequency of disk accesses, saving more power and noise, which are all stated goals of Sukegawa (column 10, lines 13-18).

To reiterate, Sukegawa queues up new or updated data in the nonvolatile cache. Once the number of new or updated data reaches a certain level, the disk is spun up and the new or updated data is written to the disk. This queuing of new, updated, or "dirty" data reduces the number of disk accesses required because instead of accessing

the disk once for each piece of new data, the disk is accessed once for a group of new data. Reducing the number of disk accesses reduces the power consumed by the disk and reduces the noise generated by the disk, since each time the disk is accessed it must be spun up, generating noise and consuming power.

What Sukegawa does not explicitly teach but what would have been obvious to the skilled artisan is that whenever a read memory request cannot be satisfied from the nonvolatile cache, the disk must be spun up to read the data, and while the disk is still spun up, it is obvious to write to the disk any data that has been queued up. The stated purpose of Sukegawa in queuing data is to reduce the frequency of disk access, thereby reducing power consumed and noise generated, and emptying the queue whenever the disk is spun up to satisfy a read request further reduces the frequency of disk access since it delays any future need to spin the disk up due to a full queue needing to be emptied to the disk. In other words, the need for a future disk access to empty out the queue is delayed because it takes longer to fill the queue from empty than from partially filled. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to execute Sukegawa's queued memory requests when the hard disk is accessed in response to a read memory request.

Regarding claim 3, Sukegawa's memory controller processes digital signals and is therefore a digital signal processor. If Applicants dispute this interpretation of DSP, then specific reference must be made to the specification to show why this interpretation of DSP is inappropriate.

Regarding claim 4, Sukegawa's memory controller is an integrated circuit with a specific application (controlling memory) and is therefore an ASIC. If Applicants dispute this interpretation of ASIC, then specific reference must be made to the specification to show why this interpretation of ASIC is inappropriate.

Regarding claims 5, 32, and 33, Sukegawa does not teach that his cache system controller comprises software running on a host processor. However, he shows a host processor as host system 4 in Fig. 1 and it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the cache system controller in software to make it more flexible, upgradeable, etc.

Regarding claim 6, Sukegawa 's memory controller resides with the cache in the apparatus of Fig. 1.

Regarding claim 7, Sukegawa's memory controller is shown separate from the cache and the hard disk as claimed.

Regarding claims 10, 11, 22, and 23, Sukegawa teaches that queuing up memory writes reduces the frequency of access to his disk drive thereby saving power at column 10, lines 5-17. Furthermore, at column 7, lines 8-12 he explicitly teaches that the BIOS can start the system without activating the disk drive, thereby saving power.

From these two passages, it is clear that in some situations, accessing Sukegawa's hard disk comprises spinning up the hard disk first, as claimed.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to spin down the hard disk whenever activity was low to save power. The question of when to spin it down is a design choice taking into account power savings vs. performance degradation. In any case, once the disk is spun down, further accesses to the disk require it to be spun up first, as claimed.

Regarding claims 12, 13, 24, 25, 44, 86, 89, 92, 100, and 104, Sukegawa does not mention prefetches, but Official Notice is taken that prefetching was well-known in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement prefetching in Sukegawa's device to improve system operation by fetching data before it was needed to reduce operation time (the known benefit of prefetching).

One of the more effective uses of prefetching is for sequential streams. Once a processor determines that a request is part of a sequential stream, prefetching is implemented to obtain subsequent data of the sequential stream before it is actually needed so that when it is actually needed, it already resides in the cache and can be accessed quickly from the cache. If a request is not part of a sequential stream, prefetching may or may not be useful (overly aggressive prefetching results in storing data in the cache that will never be used, forcing data in the cache that would have been used again to be thrown out). Prefetching is always a design tradeoff between

gaining the speed advantage of having prefetched data in the cache before it is actually requested and throwing out data that will be used again to make room for prefetched data that might not be used. The small size of a cache is what makes prefetching potentially more detrimental than beneficial to operating speed.

Regarding claims 14, 18, and 53, Sukegawa does not teach determining if queued operations are desirable and then performing only the operations that are desirable. However, Official Notice is taken of queue operation techniques whereby more recent queue entries make older queue entries obsolete and therefore undesirable. Those undesirable queue entries are then deleted to avoid wasted operations. This typically includes memory requests to the same address where a first write to a certain address is made obsolete by a later write to the same address, for example. Since the first write is still in the queue (and has therefore not been written to memory) when the second write to the same address is placed in the queue, the first write can be deleted with no consequence to program operation as long as there are no intervening reads to that same address.

Regarding claims 40, 41, 43, 45, 46, 48, 49, 51, and 60, Sukegawa's device clearly can begin operation without spinning up the hard disk as discussed in the rejection of claim 10. His BIOS reads the necessary data from the flash memory to boot up the machine and get the operating system and one or more application programs up

and running. Furthermore, he clearly teaches queuing first access requests (new data writes) as discussed in the rejection of claim 1.

What he doesn't say but what is readily apparent is that once certain access requests (such as reads) are received that cannot be satisfied from the flash memory, the hard disk must be spun up to satisfy the requests. What is obvious is that once the disk is then spun up, the queued requests can quickly and efficiently be "unqueued" or sent to the disk, completing them as claimed.

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Claims 2, 54, 55, 57, 59, 77, 82, 83, 84, 88, 90, 91, 94, 95, 97, 98, 102, 103, 105, and 106 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,860,083 to Sukegawa in view of the IBM Technical Disclosure Bulletin NN9411421 published 11/1/94, hereinafter simply the TDB.

Sukegawa does not teach that his non-volatile memory is a polymer ferroelectric memory, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to make it so for the attendant advantages of polymer ferroelectric memory.

The TDB teaches that it was known to use polymer ferroelectric memories for nonvolatile storage purposes. As taught by the TDB, polymer ferroelectric memory was a known type of nonvolatile memory at the time of the invention and it therefore would

have been an obvious choice to use for the nonvolatile memory in Sukegawa's device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a polymer ferroelectric memory for the design benefits that it provides, including small size, inexpensive construction, and fast response times.

Additionally regarding claim 55, the grounds of rejection of the other independent claims is relevant but is not repeated here for brevity. Similarly, the grounds of rejection of the parent claims of the dependent claims in this section are not repeated here for brevity.

Response to Arguments

Applicant essentially has only one argument: that Sukegawa does not teach "that updated data in non-volatile cache area 10C is updated to HDD 2 in response to a read request, read operation, or cache read miss" (page 17, first full paragraph). In other words, Applicant is asserting that Sukegawa does not teach sending cached data to the disk in response to a read that misses the cache.

First of all, it is noted that it is quite true that Sukegawa does not teach sending cached data or queued data to the disk in response to a cache read miss. In fact the Examiner had stated that this technique was not disclosed by Sukegawa but rather was obvious in view of Sukegawa. Note the Office action at page 3, lines 3-8 and page 6, lines 8-12 as cited by the Applicant.

While it is true that Sukegawa does not explicitly teach sending cached data to the disk upon a cache read miss, such a step would have been obvious to one of ordinary skill in the art at the time the invention was made as argued above. Clearly Sukegawa teaches queuing updated data. This is data that is new or "updated" and has not been stored to the disk yet. It is queued up so that it can be written back to the disk eventually. It is queued up and written to the disk at a later time with other updated data to save power by reducing the number of times the disk has to be spun up. Clearly there is a power savings achieved by queuing the data in the nonvolatile cache since the disk is spun up less often and for a shorter total amount of time.

Then once the disk must be spun up, such as when a cache read miss occurs (meaning a read request has not located the desired data in the cache), the updated data that is in the queue can obviously be written back to the disk while it is still spun up for the read request. The alternative, which Applicant seems to suggest, is that Sukegawa's device only writes data back to the disk when the queue is full. Clearly Sukegawa's device must write data back to the disk when the queue is full (or perhaps as late as when the queue is full and there is one more write request which cannot fit in the queue), but to suggest it wouldn't be obvious to also empty the queue by writing back the updated data therein every time the disk is spun up for satisfying a read request is not persuasive. The skilled artisan reading Sukegawa's disclosure is keenly aware of the desire to save power since Sukegawa mentions this desire, and emptying the queue by writing back updated data when the disk is spun up to satisfy a cache read miss is a clear opportunity to save additional power by delaying any future need to spin

the disk up due to a full queue needing to be emptied to the disk because it takes longer to fill the queue from empty than from partially filled.

Applicant's attention is directed to U.S. Patent 5,636,355 to Ramakrishnan et al., column 6, lines 5-60 where one known example of writing queued requests to a disk upon a read access is disclosed. This patent was cited in the international search report for the application PCT/US02/31892 which claims priority from the instant application and was cited in the Information Disclosure Statement filed on 5/12/03. So while Sukegawa may not explicitly disclose the technique of storing queued writes to disk when the disk is accessed to service a read miss, clearly the technique was well-known at the time of the invention. This fact should be carefully reviewed when Applicant considers how to amend the claims in response to this final Office action.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (571) 272-4214.

Any response to this action should be labeled appropriately (including serial number, Art Unit 2189, and type of response) and mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, hand-carried or delivered to the Customer Service Window at Randolph Building, 401 Dulany Street, Alexandria, VA 22313, or faxed to (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

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Art Unit 2189